ARJUN TYAGI

Urbana, IL · arjuntyagi.cs.illinois.edu · arjun25@illinois.edu · 217-721-2414

SUMMARY

Ph.D. student in computer architecture focused on memory systems, processing-in-memory, and fast architectural simulation. Experience spanning device modeling, RTL-level design, and system-level performance, power, and reliability analysis for emerging memory technologies.

EDUCATION

University of Illinois Urbana-Champaign **Champaign, IL**
Ph.D. in Computer Science *Aug. 2024 - Present*
· GPA: 3.84/4.0

Birla Institute of Technology & Science, Pilani **Goa, India**
Bachelor of Engineering in Electronics and Instrumentation Engineering *Aug. 2019 - May 2023*
· GPA: 8.99/10.0

PUBLICATIONS, PREPRINTS & TUTORIALS

Arjun Tyagi and Shahar Kvatinsky, *Assessing the Performance of Stateful Logic in 1-Selector-1-RRAM Crossbar Arrays*, 2024 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1-5, doi: 10.1109/ISCAS58744.2024.10558539

Ben Feinberg, T. Patrick Xiao, Minh S. Q. Truong, **Arjun Tyagi**, Ryan Wong, Yiqiu Sun, and Saugata Ghose, *Tutorial on Simulation for Processing-Using-Memory Systems*, 2024 IEEE International Symposium on Computer Architecture (ISCA)

Arjun Tyagi, Minh S. Q. Trung, Ankit Shukla, Shaloo Rakheja, and Saugata Ghose, *[Title Redacted]*, Submitted to 2026 ACM/IEEE Design Automation Conference (DAC)

Arjun Tyagi and Shubham Sahay, *[Title Redacted]*, Submitted to 2026 IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), preprint available upon request

RESEARCH EXPERIENCE

ARCANA Research Group, PI: Prof. Saugata Ghose **Urbana, IL**

Rapid, Accurate Chip-Scale Simulation of Digital Compute Using Emerging Memory Devices *Sept. 2023 - present*

- Developed a chip-scale architectural simulation framework for digital processing-in-memory, achieving $> 10,000\times$ speedup over SPICE while preserving timing and power accuracy.
- Designed performance optimizations (memoization, dynamic time stepping) to scale device-aware simulation to large arrays, reducing runtime and memory footprint while preserving robustness to device variability.
- Integrated Verilog-A device models into an architectural simulation flow, enabling iterative co-design across device, circuit, and system levels.
- Implemented power, thermal, and reliability models to analyze performance degradation and lifetime effects in emerging memory-based compute systems.

ASIC^2 Research Group, PI: Prof. Shahar Kvatinsky **Haifa, Israel**

Assessing the Performance of Stateful Logic in 1-Selector-1-RRAM Crossbar Arrays *Jan. - Jun. 2023*

- Developed a compact Verilog-A model for 1S1R memory cells to enable large-scale architectural and circuit-level simulations.
- Modeled parasitic RC effects in crossbar interconnects to quantify array-size-dependent latency, energy, and signal degradation.

- Evaluated passive (1R) and active (1S1R) RRAM crossbar arrays (4×4 to 512×512) for in-memory logic, demonstrating up to 24.4× lower power and 4.5× higher readout margin with 1S1R designs.

CtrlPIM: A Microcode-Based Controller for Memristive Memory Processing Unit *Jan. - Jun. 2023*

- Co-designed a microcode-based memory controller and PIM ISA for a memristive memory processing unit (mMPU), targeting system-level integration.
- Implemented and validated the controller on a Xilinx Zynq-7000 FPGA platform.

NeuroChaSe Group, PI: Prof. Shubham Sahay **Kanpur, India**

Efficient Reinforcement Learning on Passive RRAM Crossbar Array *Jan. - Jul. 2022*

- Performed an algorithm-hardware co-design and proposed a novel implementation of Monte Carlo reinforcement learning algorithm on passive RRAM crossbar array.
- Demonstrated $> 100,000\times$ area reduction over prior digital and 1T1R-based implementations, while maintaining robustness to spatial/temporal variations and endurance failures in RRAM devices.

AWARDS & SCHOLARSHIPS

- **First-Year Ph.D. Fellowship** *Aug. 2024 - May 2025*
  University of Illinois Urbana-Champaign
- **Summer Undergraduate Reseach Internship** *May - Aug. 2022*
  Arizona State University
- **Summer Research Fellowship Programme** *May - Aug. 2022*
  Indian Institute of Technology Delhi

SKILLS

- **Programming & Modeling**: C, C++, Python, OpenMP, MATLAB, Verilog HDL, Verilog-A
- **Computer Architecture & Systems**: Memory hierarchy, processing-in-memory, memory controllers, architectural simulation, performance modeling, power and thermal analysis, reliability modeling
- **Hardware & RTL**: RTL design and simulation, FPGA-based prototyping, microcode-based controllers
- **Tools & Platforms**: Linux, Git, Xilinx Vivado, FPGA SoCs (Zynq-7000), SPICE

TUTORING & VOLUNTEERING EXPERIENCE

- **Graduate Student Ambassador at UIUC CS** *Mar. 2025*
- **Undergraduate/Graduate Mentor**, UIUC
  · Dylan Meeks, BS ECE '26 at University of Texas at Austin *Jun. - Aug. 2025*
  · Qingyuan Liu, MS ECE '26 at University of Illinois Urbana-Champaign *Aug. 2025 - present*

TEACHING EXPERIENCE

- **ECE 313: Analog & Digital VLSI Design** **BITS Pilani**
  Undergraduate Teaching Assistant *Aug. - Dec 2022*
- **ECE 241: Microprocessor & Interfacing** **BITS Pilani**
  Undergraduate Teaching Assistant *Jan. - May 2022*
- **ECE 216: Digital Design** **BITS Pilani**
  Undergraduate Teaching Assistant *Aug. - Dec 2021*